Reg.No. \_\_\_\_\_\_\_\_\_\_\_\_



**End Semester Examination – Nov/Dec – 2018**

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| **Code :** | **18EI3002** | **Duration :** | **3hrs** |
| **Sub. Name :** | **EMBEDDED SYSTEM AND SOFTWARE DESIGN** | **Max. marks :** | **100** |

**ANSWER ANY FIVE QUESTIONS (5 x 16 = 80 Marks)**

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| **Q. No.** | **Sub Div.** | **Questions** | **Course**  **Outcome** | **Marks** |
| 1. | a. | Explain ARM processor, architecture, instruction set programming. | CO1 | 12 |
| b. | In what ways CISC and RISC processors differ? | CO1 | 2 |
| c. | What are the points to be considered while connecting power supply rails with embedded system? | CO1 | 2 |
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| 2. | a. | Draw the data frame format of CAN? | CO2 | 4 |
| b. | Discuss the I/O devices & its interfacing concepts? | CO2 | 12 |
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| 3. | a. | Explain in detail the various scheduling policies with example. | CO3 | 10 |
| b. | Enumerate on inter process communication. | CO3 | 6 |
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| 4. | a. | Analyse the role of UML in OO design. | CO4 | 10 |
| b. | What do you mean by DAG. | CO4 | 3 |
| c. | Tabulate the advantages and disadvantages of debug kernel. | CO4 | 3 |
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| 5. | a. | Write an 8051 C program to toggle all the bits of port P1 continuously with some delay in between. Use Timer 0, 16-bit mode to generate the delay. | CO5 | 8 |
| b. | Outline how data is transferred serially in embedded controllers. | CO5 | 8 |
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| 6. | a. | Enlist the steps involved in various methods of data transfers in DMA. | CO1 | 10 |
| b. | Sketch the organization of various structural units in a processor. | CO1 | 6 |
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| 7. |  | Write the fifteen point strategy for synchronization between the ISRs, OS functions and tasks for resource management. | CO2 | 16 |
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| **COMPULSORY QUESTION (1 x 20 = 20 Marks)** | | | | |
| 8. | a. | Sketch the class diagram and mention the requirements for a smart card. | CO6 | 10 |
| b. | List out the stages of product lifecycle model. | CO6 | 10 |